UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/529,503	10/25/2005	Masaki Kitaoka	SUGI-101US	6154

23122 7590 12/04/2009
RATNERPRESTIA
P.O. BOX 980
VALLEY FORGE, PA 19482

EXAMINER	
MCCOMMAS, STUART S	
ART UNIT	PAPER NUMBER
2629	
MAIL DATE	DELIVERY MODE
12/04/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/529,503	KITAOKA ET AL.	
	Examiner	Art Unit	
	Stuart McCommas	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (United States Patent 6,268,840), hereinafter referenced as Huang, in view of Mi et al. (United States Patent 6,894,668), hereinafter referenced as Mi.

Regarding claim 1, Huang discloses a method for driving a cholesteric liquid crystal display device in which a cholesteric liquid crystal is driven in a matrix manner by means of a plurality of common electrodes (1162) and segment electrodes (1182), the common electrodes and segment electrodes being crossed oppositely (figure 2), the method comprising the steps of:

writing display content to the cholesteric crystal by sequentially applying common electrode drive voltage waveforms from the common electrodes (1162) to the cholesteric liquid crystal display device, the common electrode drive voltage waveforms including a reset voltage waveform to cause the cholesteric liquid crystal to enter a homeotropic state, a select voltage waveform to select a final alignment state of the cholesteric liquid crystal, a hold voltage waveform to hold an alignment state selected by the select voltage waveform, and a non-select voltage waveform caused by a matrix drive (column 5 lines 6-67; column 6 lines 1-4; column 6 lines 26-67; column 7 lines 1-

20; figures 3A-3B; figures 4A-4F; figures 6A-6D; figure 7).

applying segment electrode drive voltage waveforms from the segment electrodes (1182) to the cholesteric liquid crystal display device during the step of writing the display content, the segment electrode drive voltage waveforms including at least an ON voltage waveform for determining the final alignment state of the cholesteric liquid crystal as a planar alignment state (figures 6A-6D), and an OFF voltage waveform for determining the final alignment state as a focal conic state (column 5 lines 60-67; column 6 lines 1-4; figures 3A-3B; figures 6A-6D).

However Huang fails to disclose wherein the common electrode drive voltage waveforms have two levels of voltages for all of the common electrodes and all periods of time.

In a similar field of endeavor Mi discloses wherein the common or row electrode drive voltage waveforms have two levels of voltages for all of the common or row electrodes and all periods of time (column 3 lines 6-23; column 7 lines 15-61; column 8 lines 21-55; column 11 lines 29-60; figure 1; figures 4-8).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Huang with Mi by specifically providing that the common voltage levels have two levels of voltages for all of the common electrodes and all periods of time for the purpose of only using two voltage levels to minimize the number of voltages required to precisely control the display (column 3 lines 23-30).

Regarding claim 2, Huang and Mi, the combination discloses everything as applied above, further Huang discloses that each of the reset, select, hold, non-select,

ON and OFF voltage waveforms has the same number of unit intervals (figures 6A-6D), and each of the reset, select, hold, non-select voltage waveforms has two levels of voltages in the same unit interval (figures 6A-6D), and each of the ON and OFF voltage waveforms has two or less levels of voltages in the same unit interval (figures 6A-6D).

Regarding claim 3, Huang and Mi, the combination discloses everything as applied above, further Huang discloses that each of the reset, select, hold, and non-select voltage waveforms has two levels of voltages (figures 6A-6D).

Regarding claim 4, Huang and Mi, the combination discloses everything as applied above, further Huang discloses that each of the reset, select, hold, and non-select voltage waveforms has three levels of voltages (figures 6A-6D).

Regarding claim 5, Huang and Mi, the combination discloses everything as applied above, further Huang discloses that each of the reset, select, hold, and non-select voltage waveforms has four levels of voltages (figures 6A-6D).

Regarding claim 6, Huang and Mi, the combination discloses everything as applied above, further Huang discloses that the maximum voltage value of the reset voltage waveform and the maximum voltage value of the hold voltage waveform are the same voltage value of 60 volts (figures 6A-6D).

Regarding claim 7, Huang and Mi, the combination discloses everything as applied above, further Huang discloses that each of the ON and OFF voltage waveforms has three or four levels of voltages (figures 6A-6D).

Regarding claim 8, Huang and Mi, the combination discloses everything as applied above, further Huang discloses that each of the ON and OFF voltage

waveforms has two levels of voltages (figures 6A-6D).

Regarding claim 9, Huang and Mi, the combination discloses everything as applied above, further Huang discloses that the ON and OFF voltage waveforms and the non-select voltage waveform applied to the columns are the same (figures 6A-6D).

Regarding claim 10, Huang and Mi, the combination discloses everything as applied above, further Huang discloses that the select and non-select voltage waveforms are the same (figures 6A-6D).

Regarding claim 11, Huang discloses a cholesteric liquid crystal display apparatus comprising:

a liquid crystal display device in which a plurality of picture elements are formed at portions crossed by a plurality of common electrodes (1162) and segment electrodes (column 4 lines 44-50; figure 2; figure 7);

a common driver (row driver 150) for writing display content to the picture elements by sequentially applying drive voltage waveforms from the common electrodes to the cholesteric liquid crystal display device (column 11 lines 8-50; figure 7), the drive voltage waveforms including a reset voltage waveform to cause the cholesteric liquid crystal to enter a homeotropic state, a select voltage waveform to select a final alignment state of the cholesteric liquid crystal, a hold voltage waveform to hold an alignment state selected by the select voltage waveform, and a non-select voltage waveform caused by a matrix drive, wherein the common drive concurrently applied each of the reset, select, hold and non-select waveforms to respectively different portions of the common electrodes (column 5 lines 6-67; column 6 lines 1-4; column 6

lines 26-67; column 7 lines 1-20; figures 3A-3B; figures 4A-4F; figures 6A-6D; figure 7);

a segment driver (column driver 200) for applying drive voltage waveforms from the segment electrodes to the cholesteric liquid crystal display device during the step of writing a-the display content, the drive voltage waveforms including at least an ON voltage waveform for determining the final alignment state of the cholesteric liquid crystal as a planar alignment state, and an OFF voltage waveform for determining the final alignment state as a focal conic state (column 5 lines 60-67; column 6 lines 1-4; column 11 lines 51-64; figures 3A-3B; figures 6A-6D; figure 7);

a controller (250) for controlling the common driver and segment driver (column 12 lines 3-19; figure 7);

wherein the controller controls the common and segment driver in such a way that each of the reset, select, hold, non-select, ON and OFF voltage waveforms has the same number of unit intervals, the reset, select, hold, non-select voltage waveforms have two levels of voltages for all the common electrodes, and the ON and OFF voltage waveforms have not more than two levels of voltages for all the segment electrodes in the same unit interval (figures 6A-6D).

However Huang fails to disclose that the common voltage levels have two levels of voltages for all of the common electrodes and all periods of time.

In a similar field of endeavor Mi discloses that the common voltage levels or row voltage levels have two levels of voltages for all of the common or row electrodes and all periods of time (column 3 lines 6-23; column 7 lines 15-61; column 8 lines 21-55; column 11 lines 29-60; figure 1; figures 4-8).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Huang with Mi by specifically providing that the common voltage levels have two levels of voltages for all of the common electrodes and all periods of time for the purpose of only using two voltage levels to minimize the number of voltages required to precisely control the display (column 3 lines 23-30).

Regarding claim 12, Huang and Mi, the combination discloses everything as applied above, further Huang discloses that the controller (250) controls the common driver in such a way that there is no period of time during which the same voltage is applied to all common electrodes in a period of time from the application of the hold voltage waveform to the first common electrode to the application of the reset voltage waveform to the last common electrodes during a step of writing a-the display content (column 10 lines 33-67; column 11 lines 1-6; figures 4A-4F; figures 6A-6D), and that there is a period of time during which the same voltage is applied to all segment electrodes during the step of writing the display content (column 10 lines 16-32; figures 4A-4F; figures 6A-6D).

Regarding claim 13, Huang and Mi, the combination discloses everything as applied above, further Huang discloses that the controller (250) controls the common driver in such a way that the voltages applied to the common electrodes have two levels of voltages (figures 6A-6D).

Regarding claim 14, Huang and Mi, the combination discloses everything as applied above, further Huang discloses that the controller controls the common driver in such a way that the voltages applied to the common electrodes have three levels of

voltages Vh, Vm, and V1 (figures 6A-6D), and include, for writing a display content, a unit interval during which the voltages applied to the common electrodes include Vh and Vm (figures 6C-6D) and a unit interval during which the voltages applied to the common electrodes include Vm and V1 (figures 6A-6B).

Regarding claim 15, Huang and Mi, the combination discloses everything as applied above, further Huang discloses that the controller controls the common driver in such a way that the voltages applied to the common electrodes have three levels of voltages Vh, Vm, and V1 (figures 6A-6D), and include, for writing a display content, a unit interval during which the voltages applied to the common electrodes include Vh and V1 (figures 6A-6D) and a unit interval during which the voltages applied to the common electrodes include Vm and V1 (figures 6A-6B).

Regarding claim 16, Huang and Mi, the combination discloses everything as applied above, further Huang discloses that the controller controls the common driver in such a way that the voltages applied to the common electrodes have three levels of voltages Vh, Vmh, Vml, and V1 (figures 6A-6D), and include, for writing a display content, a unit interval during which the voltages applied to the common electrodes include Vh and V1 (figures 6A-6D), and a unit interval during which the voltages applied to the common electrodes include Vm and V1 (figures 6A-6B), and a unit interval during which the voltages applied to the common electrodes include Vmh and Vml (figures 6B-6C).

Regarding claim 17, Huang and Mi, the combination discloses everything as applied above, further Huang discloses that the controller controls the segment driver in

such a way that the voltages applied to the segment electrodes have four levels of voltages V1, V2, V3 and V4 (figures 6A-6D; figures 17-22), and include, for writing a display content, a unit interval during which the voltages applied to the segment electrodes include V1 (figure 17), and a unit interval during which the voltages applied to the segment electrodes include V1 and V2 (figures 17-22), and a unit interval during which the voltages applied to the segment electrodes include V3 and V4 (figures 17-22).

Regarding claim 18, Huang and Mi, the combination discloses everything as applied above, further Huang discloses that the controller controls the segment driver in such a way that the voltages applied to the segment electrodes have three levels of voltages V1, V2, and V4 (figures 6A-6D; figures 17-22), and include, for writing a display content, a unit interval during which the voltages applied to the segment electrodes include V1 (figures 6A-6D; figures 17-22), and a unit interval during which the voltages applied to the segment electrodes include V2 and V4 (figures 17-22).

Regarding claim 19, Huang and Mi, the combination discloses everything as applied above, further Huang discloses that the controller controls the segment driver in such a way that the voltages applied to the segment electrodes have three levels of voltages V1, V2, and V4 (figures 6A-6D; figures 17-22), and include, for writing a display content, a unit interval during which the voltages applied to the segment electrodes include V4 (figures 6A-6D; figures 17-22), and a unit interval during which the voltages applied to the segment electrodes include V1 and V2 (figures 17-22).

Regarding claim 20, Huang and Mi, the combination discloses everything as applied above, further Huang discloses that the controller controls the segment driver in

such a way that the voltages applied to the segment electrodes have three levels of voltages V1, V2, and V4 (figures 6A-6D; figures 17-22), and include, for writing a display content, a unit interval during which the voltages applied to the segment electrodes include V2 (figures 6A-6D; figures 17-22), a unit interval during which the voltages applied to the segment electrodes include V4 (figures 6A-6D; figures 18-22), and a unit interval during which the voltages applied to the segment electrodes include V1 and V2 (figures 6A-6D; figures 17-22).

Regarding claim 21, Huang and Mi, the combination discloses everything as applied above, further Huang discloses that the controller controls the segment driver in such a way that the voltages applied to the segment electrodes have three levels of voltages V1, V2, and V4 (figures 6A-6D), and include, for writing a display content, a unit interval during which the voltages applied to the segment electrodes include V1 (figures 6A-6D), a unit interval during which the voltages applied to the segment electrodes include V2 (figures 6A-6D), a unit interval during which the voltages applied to the segment electrodes include V4 (figures 6A-6D), and a unit interval during which the voltages applied to the segment electrodes include V2 and V4 (figures 6A-6D; figures 17-22).

Regarding claim 22, Huang and Mi, the combination discloses everything as applied above, further Huang discloses that the controller controls the segment driver in such a way that the voltages applied to the segment electrodes have four levels of voltages V1, V2, and V4 (figures 6A-6D), and include, for writing a display content, a unit interval during which the voltages applied to the segment electrodes include V1

(figures 6A-6D), a unit interval during which the voltages applied to the segment electrodes include V4 (figures 6A-6D), and a unit interval during which the voltages applied to the segment electrodes include V2 and V4 (figures 6A-6D; figures 17-22).

Regarding claim 23, Huang and Mi, the combination discloses everything as applied above, further Huang discloses that the controller controls the segment driver in such a way that the voltages applied to the segment electrodes have two levels of voltages (figures 6A-6D; figures 17-22).

Regarding claim 24, Huang and Mi, the combination discloses everything as applied above, further Huang discloses that the controller controls the common and segment drivers in such a way that the voltages applied to the common and segment electrodes are 42 volts or less (figures 6A-6D).

Response to Arguments

3. Applicant's arguments with respect to claims 1-24 have been considered but are believed to be answered by and therefore moot in view of the new ground(s) of rejection.

On page 9 of Applicant's remarks, Applicant argues that Huang does not disclose the voltages applied to the common and segment electrodes are 42 volts or less.

The Examiner respectfully disagrees, because Huang discloses that in at least a portion of time while the display is driven the voltage applied to the common and segment electrodes is 42 volts or less (figures 6A-6D).

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stuart McCommas whose telephone number is (571)270-3568. The examiner can normally be reached on Monday-Friday 9 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexander Eisen can be reached on (571)272-7687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stuart McCommas/
Patent Examiner
Art Unit 2629

SSM

/Alexander Eisen/
Supervisory Patent Examiner, Art Unit 2629